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10/826,362	04/19/2004	Masao Murade	119293	1036

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EXAMINER	
ABDULSELAM, ABBAS I	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/826,362	MASAO MURADE	
	Examiner	Art Unit	
	Abbas I. Abdulselam	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-8 and 17-21* is/are rejected.

7)☒ Claim(s) *2,4 and 9-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 5/04/06, 1/09/06, 11/23/05, 4/19/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3, 5-8, 17-18 and 20-21 rejected under 35 U.S.C. 102(b) as being anticipated by Maruoka et al. (US 2002/0186192)

Regarding claim 1, Maruoka et al. (2002/0186192) teaches an electro-optic device *([0066], LCD)*, comprising: a substrate; *([0067], same substrate, [0168], Fig. 38 (1), driving circuit substrate (1))* data lines extending in one direction above the substrate *([0067], Fig. 1 (103), video signal lines (103))*; scanning lines extending in a direction orthogonal to the data lines above the substrate *([0067], Fig. 1 (102), scanning signal lines (102))*; switching elements *(Fig. 33 (30), active elements (30))* to which scanning signals are supplied from the scanning lines, the switching elements being disposed above the substrate *([0144], Fig. 33 (30, 102), plurality of pixel portions (101) each including an active element (30), [0067], a display part (110) includes pixel portions (101) such that the display part (110) is formed on the same substrate)*; pixel electrodes *(Fig. 33 (109), pixel electrodes (109))* to which image signals are supplied from the data lines through the switching elements *([0144], each pixel portion (101) includes the active element (30) and a*

pixel electrode (109), [0145], gray scale voltages are supplied to the video signal line (103) when active elements (30) are turned on, and gray scale voltages are supplied to pixel electrode (109) from the video signal line (103)) the pixel electrodes being disposed above the substrate *([0144], each pixel portion (101) includes a pixel electrode (109), [0067], and that the display part (110) is formed on the same substrate, note that pixel portions (101) are part of the display part (110))* the substrate having an image display area including the pixel electrodes and the switching elements, and a peripheral area at a periphery of an image display area *([0067], the display part (110) has pixel portions (101) arranged in matrix array with the pixel portions (101) including pixel electrodes (109) and active elements (30) (Fig. 33) such that the display part (110), a horizontal driving circuit (120) and vertical driving circuit (130) are formed on the same substrate)*; storage capacitors that hold an electrical potential at the pixel electrodes for a predetermined time, the storage capacitors being disposed above the image display area *([0144], Fig. 33 (115, 109), a pixel capacitance (115) is connected to the pixel electrode (109), and as shown in Fig. 33, the pixel capacitance is on pixel portion (101), [0147], voltages of the pixel potential control signals applied to the electrodes of the pixel capacitance (115) from the pixel potential control circuit 135, not that it is inherent for some time to be elapsed before the pixel capacitance (115) discharges)*; first wiring *(Fig. 33 (136))* that supplies capacitor electrodes of the storage capacitors with a predetermined

electrical potential, the first wiring being disposed above the image display area *([0144], Fig. 33 (135, 115), the pixel capacitance (115) is connected to the pixel potential control line (136) which in turn is connected to pixel potential control circuit (135), [0147], voltages of the pixel potential control signals applied to the electrodes of the pixel capacitance (115) from the pixel potential control circuit 135, and as shown in Fig. 33, the pixel potential control line (136) is on pixel portion (101));* and a frame *(Fig. (39 44))* formed as the same film as the first wiring*(Fig. 33 (136))*, the frame being disposed at least a part of a frame area between the image display area and the peripheral area *([0174], it is possible to form wiring using light shielding film (44) extending from the pixel potential control circuit (135) to the pixel capacitance using a conductive layer(49) [0175], Fig. 39 (44), The first light shielding film 44 has the function of the pixel potential control lines (136) and is continuously formed., and connects to the pixel potential control circuit 135, as shown in Fig.33, part of pixel potential control lines (136) lies between a display part (110), and vertical driving circuit (130), and also between a display part (110), and a pixel potential control circuit (135)).*

Regarding claim 3, Maruoka teaches the first wiring being formed of the same film as the capacitor electrodes to which the predetermined electrical potential is supplied, the first wiring being continuous with the capacitor electrodes in a same plane *([0175], the first light*

shielding film 44 is formed such that the first light shielding film 44 covers the whole surface of the display region to perform the function as the light shielding film, to allow the light shielding film 44 to have the function of the pixel potential control lines 136, which as shown in Fig. 33 is connected to pixel potential control circuit (135) first light shielding film 44 also functions as the electrodes of the pixel capacitance).

Regarding claim 5, Maruoka teaches a counter substrate opposing the substrate *([0229], Fig. 49 (1, 2), substrate (1) and the transparent substrate 2)*; and a sealing member that bonds the substrate with the counter substrate *([0229], Fig. 49 (1, 2, 12), the driving circuit substrate (1) and the transparent substrate 2 are fixed to each other by adhesion using the sealing material 12)*; the frame being disposed at least a part of a sealing area where the sealing member is disposed *([0227], The first light shielding film 44 covers substantially the whole surface of the driving circuit substrate (1) and an opening is constituted of only a portion of* ***the contact hole 42CH in which a metal film which forms the first light shielding film 44 is part of part of lamination).***

Regarding claim 6, Maruoka teaches a counter substrate opposing the substrate *([0229], Fig. 49 (1, 2), substrate (1) and the transparent substrate 2)*; and a counter electrode disposed above the counter substrate *([0230], counter electrodes (5)*

formed on the transparent substrate (2)); the frame including a connecting portion electrically coupled with the counter electrode *([0227], The first light shielding film 44 covers substantially the whole surface of the driving circuit substrate (1) and an opening is constituted of only a portion of the contact hole (42CH) in which a metal film which forms the first light shielding film 44 is part of lamination, note that through the contact hole (42CH) on the driving circuit substrate (1), counter electrodes (5) that are formed the transparent substrate (2) would be accessed, see Fig. 39 (42CH), Fig. 49 (1, 2)).*

Regarding claim 7, Maruoka teaches the frame being formed so as to be electrically coupled with the first wiring *([0174], the first light shielding film (44) is used as the pixel potential control lines (136)).*

Regarding claim 8, Maruoka teaches the connecting portion being disposed at a corner of the counter substrate *([0227], contact hole (42CH), note the arrangements of contact holes (42CH) including in the corners as shown in Fig. 39, and clearly through the contact hole (42CH) on the driving circuit substrate (1), the transparent substrate (2) would be accessed, see Fig. 39 (42CH), Fig. 49 (1, 2)).*

Regarding claim 17, Maruoka teaches the first wiring comprising a light-shielding material *([0175], the light shielding film (44) has the function of the pixel potential control lines (136)).*

Regarding claim 18, Maruoka teaches first wiring having a layered structure comprising different materials *([0226], The first light shielding film 44 is formed of a multi-layered metal film made of tungsten and aluminum).*

Regarding claim 20, Maruoka teaches the light-shielding film comprising a frame-shaped light-shielding film disposed along an edge of the counter substrate *([0227], The first light shielding film (44) covers substantially the whole surface of the driving circuit substrate 1, note that the transparent substrate 2 is under the driving circuit substrate 1, see fig. 49 (1, 2)).*

Regarding claim 21, Maruoka teaches electronic equipment comprising the electro-optic device *([0066], an LCD device).*

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Maruoka et al. (2002/0186192).

Regarding claim 19, Maruoka teaches: a counter substrate opposing the substrate *([0229], Fig. 49 (1, 2), substrate (1) and the transparent substrate 2)*; and a light-shielding film above the counter substrate *([0227], The first light shielding film (44) covers substantially the whole surface of the driving circuit substrate 1, note that the transparent substrate 2 is under the driving circuit substrate 1, see fig. 49 (1, 2))*,

While Maruoka teaches the first light shielding film 44 is formed of a multi-layered metal film made of tungsten and aluminum [0226],

Maruoka does not specifically teach the frame being disposed so that the frame is overlapped by the light-shielding film.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to recognize the multi-layered components of the light shielding film (44) shown in Fig. 39 for the purpose of identifying the components with respect to their distinct functions as taught by Maruoka ([0175]).

Allowable Subject Matter

5. Claims 2, 4, 9, 10-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 2, Maruoka does not teach an electro-optic device with data lines, scanning lines, pixel electrode, and switching element being all disposed above a substrate, the substrate which has an image display area including pixel electrodes, the switching elements and a peripheral area, storage capacitors being disposed above the image display area, first wiring supplying electrodes of the storage capacitors, the first wiring being disposed above the image display area, a frame formed as the same film as the first wiring, the frame being disposed at least partly between the image display area and the peripheral area such that **the frame covers at least a sampling circuit that supplies the data lines with the image signals.**

Regarding claim 4, Maruoka does not teach an electro-optic device with data lines, scanning lines, pixel electrode, and switching element being all disposed above a substrate, the substrate which has an image display area including pixel electrodes, the switching elements and a peripheral area, storage capacitors being disposed above the image display area, first wiring supplying electrodes of the storage capacitors, the first wiring being disposed above the image display area, a frame formed as the same film as the first wiring, the frame being disposed at

least partly between the image display area and the peripheral area such that **the frame has at least one of separated segments as a strip having a floating potential.**

Regarding claim 9, Maruoka does not teach an electro-optic device with data lines, scanning lines, pixel electrode, and switching element being all disposed above a substrate, the substrate which has an image display area including pixel electrodes, the switching elements and a peripheral area, storage capacitors being disposed above the image display area, first wiring supplying electrodes of the storage capacitors, the first wiring being disposed above the image display area, a frame formed as the same film as the first wiring, the frame being disposed at least partly between the image display area and the peripheral area such that **the frame surrounds the entire peripheral of the image display area.**

Regarding claim 10, while Maruoka teaches image display area having a generally rectangular shape in plan view *(see Fig. 33 (110), a display part (110))*, the frame having a first pattern along three continuous sides of the rectangle *([0175], the first light shielding film (44) is formed such that the first light shielding film (44) covers the whole surface of the display region to perform the function as the light shielding film, note that excluding any one side of the display part (110) could be considered)*, and the connecting portion being disposed on the first pattern *([0227], contact hole (42CH), note the arrangements of contact holes (42CH) including in Fig. 39).*

Maruoka does not teach an electro-optic device with data lines, scanning lines, pixel electrode, and switching element being all disposed above a substrate, the substrate which has an image display area including pixel electrodes, the switching elements and a peripheral area, storage capacitors being disposed above the image display area, first wiring supplying electrodes of the storage capacitors, the first wiring being disposed above the image display area, a frame formed as the same film as the first wiring, the frame being disposed at least partly between the image display area and the peripheral area, a counter electrode disposed above a counter substrate, the frame including a connecting portion electrically coupled with the counter electrode, the frame having a first pattern along three continuous sides of a rectangular display, and **a second pattern along a remaining side of the rectangle and separate from the first pattern,** and the connecting portion being disposed on the first pattern

Regarding claim 11, while Maruoka teaches image display area having a generally rectangular shape in plan view *(see Fig. 33 (110), a display part (110))*, the frame having a third pattern along two opposing sides of the rectangle *([0175], the first light shielding film (44) is formed such that the first light shielding film (44) covers the whole surface of the display region to perform the function as the light shielding film, note that there are two sets of opposing sides of the display part (110) from which one of the two sets could be considered),* and the connecting portion being disposed on the third pattern *([0227], contact hole (42CH), note the arrangements of contact holes (42CH) including in Fig. 39).*

Maruoka does not teach an electro-optic device with data lines, scanning lines, pixel electrode, and switching element being all disposed above a substrate, the substrate which has an image display area including pixel electrodes, the switching elements and a peripheral area, storage capacitors being disposed above the image display area, first wiring supplying electrodes of the storage capacitors, the first wiring being disposed above the image display area, a frame formed as the same film as the first wiring, the frame being disposed at least partly between the image display area and the peripheral area, a counter electrode being disposed above a counter substrate, the frame including a connecting portion electrically coupled with the counter electrode such that the frame has a pattern along with two opposing sides of a rectangular display area and **another pattern along a remaining two sides of the rectangle and separate from the former pattern**, wherein the connecting portion is disposed on the former patter,

Regarding claim 12, Maruoka does not teach an electro-optic device with data lines, scanning lines, pixel electrode, and switching element being all disposed above a substrate, the substrate which has an image display area including pixel electrodes, the switching elements and a peripheral area, storage capacitors being disposed above the image display area, first wiring supplying electrodes of the storage capacitors, the first wiring being disposed above the image display area, a frame formed as the same film as the first wiring, the frame being disposed at least partly between the image display area and the peripheral area, a counter electrode being disposed above a counter substrate, the frame including a connecting portion electrically coupled with the counter electrode such that **the frame has a pattern continuously formed around a**

rectangular display except for a corner of the rectangle and another pattern is disposed at the corner and separate from the former pattern, wherein the connecting portion is disposed on at least one of the former pattern and the latter pattern.

Regarding claim 13, while Maruoka teaches external circuit-connecting terminals disposed along an edge of the substrate *([0075], Fig. 1 (131, 132), the control signal lines (131) and the video signal transmission lines (132) extended from the display control device (111) to the horizontal driving circuit (120), note that the horizontal driving circuit (120) is formed on the same substrate as other components of the display panel (100), and the lines (131, 132) are illustrated crossing the display panel as shown in Fig. 1)* the external circuit-connecting terminals being disposed above the peripheral area *([0075], Fig. 1 (131, 132), the control signal lines (131) and the video signal transmission lines (132) extended from the display control device (111) to the horizontal driving circuit (120), Note that the lines (131, 132) are illustrated crossing the display panel (100) to connect over the horizontal driving circuit (120) as shown in Fig. 1)*; and second wiring continuous with the external circuit-connecting terminals, the second wiring being disposed above the peripheral area *([0075], Fig. 1 (131, 132), the control signal lines (131) and the video signal transmission lines (132) extended from the display control device (111) to the horizontal driving circuit (120), Note that the lines (131, 132) are illustrated crossing*

the display panel (100) to connect over the horizontal driving circuit (120) as shown in Fig. 1).

Maruoka does not teach an electro-optic device with data lines, scanning lines, pixel electrode, and switching element being all disposed above a substrate, the substrate which has an image display area including pixel electrodes, the switching elements and a peripheral area, storage capacitors being disposed above the image display area, first wiring supplying electrodes of the storage capacitors, the first wiring being disposed above the image display area, a frame formed as the same film as the first wiring, the frame being disposed at least partly between the image display area and the peripheral area, external circuit-connecting terminals disposed along an edge of the substrate and above the peripheral area, second wiring continuous with the external circuit-connecting terminals, the second wiring being disposed above the peripheral area such that **at least a part of the second wiring being formed of the same film as the first wiring and being formed so as to be electrically coupled with the first wiring.**

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following arts are cited for further reference.

U.S. Pat. No. 6,791,523 to Fujita et al teach as shown in Fig. 1 a liquid-crystal device including an image display area A, a data line driving circuit 100, and a scanning line driving

circuit 200 on the element substrate of a liquid-crystal panel AA, and the liquid-crystal panel AA including a timing signal generator circuit 300 as a processing circuit external to the liquid-crystal panel AA (col. 8, lines 23-30).

U.S. Pat. No. 6,404,414 to Ishii teaches as shown in Fig. 1 a liquid crystal device substrate 1 with a built-in driving circuit employed for a liquid crystal device with a pixel section 11 having a plurality of scanning lines 20 to which scanning signals are supplied and a plurality of data lines 30 to which image signals are supplied, such that the components are arranged in a matrix pattern on a transparent substrate, which is made of glass or quartz, or a silicon substrate 10 (col. 6, lines 64-67 and col. 7, lines 1-4).

U.S. Pat. No. 6,552,758 to Koyama teaches crystalline semiconductor coating 11 is formed on a substrate 10 having an insulating surface by a known method, and a gate insulating film 12 is formed to cover the semiconductor coating 11, and a gate signal line 13 is formed thereon (see FIGS. 3A and 4A), (col. 4, lines 42-46).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abbas I. Abdulselam whose telephone number is 571-272-7685. The examiner can normally be reached on Monday through Friday from 9:00 A.M. to 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Abbas I Abdulselam
Examiner
Art Unit 2629
April 14, 2007